

**In the Claims**

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Currently Amended) A multiple-level memory cell, comprising:  
a storage element formed of several polysilicon resistors connected in series between two input/output terminals; ~~and~~  
a load in series with said resistive element, the junction point thereof forming a read terminal of the memory cell, and the respective junctions between said resistors of the storage element being accessible; and  
wherein at least certain points among said junctions of the storage element and the junction of this element with the load, are connectable, individually by a switch, either to one of said input/output terminals of the storage element, or to a terminal of application of a predetermined voltage, wherein individual programming may be performed.
2. (Canceled)
3. (Previously Presented) The cell of claim 2, wherein the ends of a same resistor are not connectable to the same terminal.
4. (Previously Presented) The cell of claim 2, wherein said switches comprise MOS transistors distributed half and half between P-channel transistors and N-channel transistors.
5. (Previously Presented) The cell of claim 1, wherein all polysilicon resistors have identical nominal values.
6. (Previously Presented) The cell of claim 1, wherein the number of possible programmable levels corresponds, at most, to the number of polysilicon resistors of the storage

element plus one.

7. (Previously Presented) The memory cell of claim 1, wherein the programming is performed by imposing, in one or several of said polysilicon resistors of the storage element, a constraint current greater than a current for which the value of this resistance exhibits a maximum.

8. (Previously Presented) The cell of claim 7, wherein said constraint current is beyond a read operating current range of the storage element.

9. (Withdrawn)

10. (Withdrawn)

11. (Withdrawn)